IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

In re Application of: DAVID W. SMITH	Group Art Unit: 2665
Serial No.: 09/225,388	Confirmation No.: 2528
Filed: JANUARY 5, 1999	Examiner: Toan D. Nguyen
	Atty. Dkt.: 2000.002500/TT2581
For: METHOD AND APPARATUS FOR PATTERN MATCHING ON SINGLE AND MULTIPLE PATTERN STRUCTURES	CUSTOMER NO. 23720

APPEAL BRIEF

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

On September 8, 2008, Appellant filed a Notice of Appeal in response to a Final Office Action dated June 6, 2008, issued in connection with the above-identified application. Additionally, Appellant filed a Pre-Appeal Brief Request for Review. On November 17, 2008, the Office issued a Notice of Panel Decision from Pre-Appeal Brief Review rejecting Appellant's arguments. Therefore, Appellant hereby submits this Appeal Brief to the Board of Patent Appeals and Interferences. The date for filing this Appeal Brief, with a request for extension of two-months is March 17, 2009, and since this response is being filed within that date, this paper is timely filed.

An extension of time is required to enable this paper to be timely filed and there is no separate Petition for Extension of Time filed herewith, therefore, this paper is to be construed as also constituting a Petition for Extension of Time Under 37 CFR § 1.136(a) for a period of two-months, up to and including March 17, 2009, to enable this document to be timely filed.

The Commissioner is authorized to deduct the two-months extension fee ($450) and the fee for filing this Appeal Brief ($540.00) from Williams Morgan & Amerson, P.C. Deposit Account No. 50-0786/2000.002500. No other fee is believed to be due in connection with the filing of this document. However, should any fee under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to this document, the Commissioner is hereby authorized to deduct said fee from Williams Morgan & Amerson, P.C. Deposit Account No. 50-0786/2000.002500.

I. REAL PARTY IN INTEREST

The present application is owned by Advanced Micro Devices, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellant is not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF CLAIMS

Claims 1-35 remain pending in this application, each of which was rejected as follows:

- Claims 1-2, 9, 23-24, 31-32 and 34 are rejected under 35 U.S.C. § 101(a) as being unpatentable over U.S. Patent No. 5,802,305 ***(McKaughan)***, in view of U.S. Patent No. 5,748,688 ***(Kim)***;
- Claims 3-6, 8, 10-18, 20-22, 25-28, 30, 33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***McKaughan*** in view of ***Kim*** further in view of U.S. Patent No. 4,516,201 ***(Warren)***; and
- Claims 7, 19 and 29 are objected to as being dependent upon a rejected base claim.

Appellants appeal each of the rejections. For the convenience of the Office, Appellants identify the claims in this appeal as claims 1-35.

IV. STATUS OF AMENDMENTS

After the Final Rejections, no other amendments were made to any other claims.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention provides a method for detecting and decoding data to wake up a host circuitry (150), as provided by independent claim 1. A set of data signals is received from an external data source (110). A size of said received set of data signals is detected to use as a factor for decoding said data. The received set of data signals is decoded. A destination address from said set of data signals is extracted. The destination address extracted from said data signals is compared to a known data value. A determination is made as to whether said received data signals should be received by a host circuitry (150) based upon said comparison of said destination address extracted from said data signals to said known data value. At least one status signal alerting said host circuitry (150) of said determination that said received data signals should be received by said host circuitry (150) is generated. The host circuitry (150) is awakened from a sleep mode upon a determination that said received set of data is addressed to said host circuitry (150). *See* Figure 1; Specification, page 9, lines 1-19; page 10, lines 15-23.

The present invention also provides an apparatus for detecting and decoding data to wake up a host circuitry (150), as provided by independent claim 10. The apparatus includes means for receiving a data signal and means for detecting a size of said received data signal. The apparatus also includes a data formatter (220), a clock divider (230), a counter (240), and a host circuitry interface (245) capable of transmitting and receiving data from a host circuitry (150). The host circuitry (150) enters a wake up state from a sleep mode based upon decoded address

data received by said host circuitry (150). The decoded address data is based upon a content of said data signal and said size of said received data signals. The apparatus also includes a memory circuitry (250), a plurality of comparators (260), a mask circuitry (270), a digital logic circuitry (265), a plurality of status registers (280), and a plurality of clocked registers (285). *See* Figures 2 and 3; Specification, page 10, line 24-page 12, line 16.

The present invention also provides a computer readable program storage device encoded with instructions that, when executed by a computer, performs a method for detecting and decoding data to wake up a host circuitry (150), as provided by independent claim 23. The method includes: receiving a set of data signals from an external data source (110); detecting a size of said received set of data signals to use as a factor for decoding said data signals; decoding said received set of data signals; extracting a destination address from said set of data signals; comparing said destination address extracted from said data signals to a known data value; determining whether said received data signals should be received by a host circuitry (150) based upon said comparison of said destination address extracted from said data signals to said known data value; generating at least one status signal alerting said host circuitry (150) of said determination that said received data signals should be received by said host circuitry (150); and waking up said host circuitry (150) from a sleep mode upon a determination that said received set of data is addressed to said host circuitry (150). *See* Figure 1; Specification, page 9, lines 1-19; page 10, lines 15-23.

The present invention provides a method for detecting and decoding data to wake up a host circuitry (150), as provided by independent claim 32. A data signal is received. A size of said received data signal is detected to use as a factor for extracting a destination address. The destination address is extracted based upon said data signal to determine whether a host circuitry (150) is being addressed by comparing said destination address to a predetermined address. The

host circuitry (150) is woken from a sleep mode based upon said determination that said host circuitry (150) is being addressed. *See* Figure 1; Specification, page 9, lines 1-19; page 10, lines 15-23.

The present invention provides an apparatus for detecting and decoding data to wake up a host circuitry (150), as provided by independent claim 34. The apparatus includes a controller (130) that is adapted to: receive a data signal; detect a size of said received set of data signals to use as a factor to extract a destination address; extract said destination address based upon said data signal to determine whether a host circuitry (150) is being addressed by comparing said destination address to a predetermined address; and wake up said host circuitry (150) from a sleep mode based upon said determination that said host circuitry (150) is being addressed. *See* Figures 1 and 3; Specification, page 9, lines 1-19; page 12, line 18-page 15, line 18; page 17, line 9-page 19-, line 12.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

- Whether claims 1-2, 9, 23-24, 31-32 and 34 are rejected under 35 U.S.C. § 101(a) as being unpatentable over U.S. Patent No. 5,802,305 ***(McKaughan)***, in view of U.S. Patent No. 5,748,688 ***(Kim)***; and
- Whether claims 3-6, 8, 10-18, 20-22, 25-28, 30, 33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***McKaughan*** in view of ***Kim*** further in view of U.S. Patent No. 4,516,201 ***(Warren)***.

VII. ARGUMENT

The present invention is directed to detecting and decoding data for waking up a host circuitry from a sleep mode. The present invention provides for receiving data signals from an external source and detecting the size of the received set of data signal for use as a factor for decoding the data. Upon decoding the data, destination address is extracted from the data signals

and the destination address is compared to a known data value. The present invention provides for determining whether the received data signals should be received by a host circuitry based upon this comparison. A status signal alerting the host circuitry of the determination that the data signal should be received by the host circuitry is generated. The present invention provides for waking up the host circuitry from a sleep mode based upon a determination that the received set of data is addressed to the host circuitry. The Examiner relies heavily on U.S. Patent No. 5,802,305 (***McKaughan***) and U. S. Patent No. 5,748,688 *(**Kim**)*. However, the Examiner has failed to provide a *prima facia* showing of obviousness of the claims of the present invention based upon the cited prior art. ***McKaughan*** refers to a computer network that contains a plurality of interconnected computers, wherein a network interface card associated with the sleeping computers detects incoming packets and compares the incoming packets to a list of packets stored in the interface cards. However, ***McKaughan*** does not disclose detecting the size of the received set of data signals to use as a factor for decoding the data, as called for by claims of the present invention. ***Kim*** does not make up for this deficit. ***Kim*** discloses that the detection of the size of the data is made to perform a bit pattern detection process, and not for decoding purposes. Contrary to Examiner's arguments, ***Kim*** explicitly provides that the detection of the size of the data is made only to perform a bit pattern detection process. Therefore, neither ***McKaughan*** nor ***Kim*** discloses detecting the size of the data for use as a factor for decoding data. Additionally, there are various other elements of claims of the present invention that are not disclosed by the cited prior art.

The specific claims of the present invention are discussed below.

A. Claims 1-2, 9, 23-24, 31-32 and 34 Are Not Rendered Unpatentable under 35 U.S.C. § 103(a) by *McKaughan* (U.S. Patent No. 5,802,305) in view of *Kim* (U.S. Patent No. 5,748,688)

McKaughan, ***Kim***, or their combination fail to teach or suggest all of the elements of claims 1-2, 9, 23-24, 31-32 and 34. ***McKaughan*** simply does not disclose detecting the size of the received set of data signals in the context of determining whether the received data signal should be received by the host circuit and waking up the whole circuitry as called for by claim 1 of the present invention. ***McKaughan*** merely refers to filtering the incoming packet, comparing the resulting filtered incoming packet to the corresponding packet in a list stored on a network interface card and making a decision whether to wake up the computer. *See* Figure 4 and col. 8, lines 45-47, col. 9, lines 3-13 of ***McKaughan***. ***McKaughan*** does not disclose detecting the size of the received set of signals when determining whether to wake up the computer, which is an element called for by claim 1. Further, ***Kim*** does not make up for the deficits of ***McKaughan***.

In a previous Office Action (dated November 28, 2007), the Examiner admitted that ***McKaughan*** did not disclose detecting a size of the received set of data signals to use as a factor for decoding the data. Appellant respectfully asserts that the Examiner is correct in the statement but further submit that ***McKaughan*** does not disclose or make obvious other elements of claim 1 of the present invention. Regarding detecting the size of the data received, ***Kim*** does not make up for this deficit. The Examiner simply point to the Abstract of ***Kim*** to argue obviousness of the element of detecting a size of the received set of data signals to use as a factor for decoding the data. However, neither this portion of any other portion of discloses detecting a size of the data to use as factor for decoding the data.

In the Final Office Action dated June 6, 2008, the Examiner promotes the argument that a bit pattern detector is detected by ***Kim***. The Examiner, in the Final Office Action, also asserts that a size of the bit stream input is also disclosed by ***Kim***. However, as elaborated further

below, ***Kim*** does not disclose detecting the size of the data for decoding purposes. In fact, ***Kim*** is explicit in indicating that the detection of the size of the data is made only to perform a bit pattern detection process. Therefore, ***Kim*** does not disclose an enabling disclosure that would anticipate the detection of the size of a bit stream as called for by claims of the present invention.

Further, ***Kim*** differentiates the data pattern detection process with a separate decoding function. In other words, the fact that ***Kim*** discloses detecting the size of the data to perform a first function, *i.e.*, a bit pattern detection process, as well as the fact that ***Kim*** differentiates explicitly between the first function and a second function, *i.e.,* decoding process, clearly indicates that the detection of the size of the data performed by ***Kim*** is not directed to performing for the second function. In other words, ***Kim*** simply does not disclose detecting the size of the data to perform a detection process, as called for by claims of the present invention. Further, as described in detail below, ***McKaughan*** does not disclose detecting the size of the data. Therefore, neither cited prior art discloses at least this element of claims of the present invention. Further, various other elements are also not made obvious by the cited prior art as elaborated below.

Moreover, the Examiner, in the Final Office Action, did not address various arguments provided by the Appellant with regard to the lack of disclosure of ***Kim*** and ***McKaughan***. As described herein, the combination of ***Kim*** and ***McKaughan*** does not make obvious all of the elements of claims of the present invention. ***McKaughan***, which is the primary reference, does not disclose or make obvious several elements of claim 1 of the present invention, and ***Kim*** does not make up for the deficit of ***McKaughan***. ***McKaughan*** refers to a computer network that contains a plurality of interconnected computers, wherein a network interface card of sleeping computers detects an incoming packet and compares the incoming packet to a list of packets stored on the network interface cards. ***McKaughan*** then compares the received packet to a list

of packets on the card and provides a wake-up sequence of a remote computer (see column 6, lines 43-64 of ***McKaughan***). However, ***McKaughan*** does not disclose detecting the size of the received set of data signals as called for by claim 1 of the present invention. ***McKaughan*** merely discloses detecting an incoming packet over a network and filtering the incoming packet with a comparison mask. This does not make obvious the element of detecting the size of the received set of signals or other elements of claim 1. ***McKaughan*** does not disclose detecting the size of the received set of signals. Therefore, Appellant respectfully asserts that among other elements, ***McKaughan*** simply does not disclose or make obvious the element of detecting the size of the received set of signals when determining whether to wake up the computer.

Kim discloses that the detection of the size of the data is made to perform a bit pattern detection process, and not for decoding purposes. *See* Abstract, col. 2, line 55-col. 3, line 8; Fig. 2. The size of the data is detected to determine the position of the bit pattern to be matched. *Id.* However, ***Kim*** does not disclose detecting the size of the data for any type of decoding purpose. In fact, ***Kim*** discloses that the pattern matching function, in which size of the data is detected, is a separate function from performing a decoding function. ***Kim*** explicitly discloses that after the input data stream is converted from serial to parallel format, it is sent to two different functions: a pattern matching function (in which the size of the data is detected)—"bit pattern detector" 200, and a decoding function—"Code Table" 330. *See* Fig. 3; col. 5, line 53-col. 6, line 4. Therefore, ***Kim*** explicitly discloses that detection of the size of the data is not used as any type of a factor for decoding the data, but is simply used to performing pattern matching. Further, ***Kim*** explicitly makes clear that the pattern matching function is different from the decoding function. Therefore, ***Kim*** fails to make obvious at least the element of detecting a size of the received set of data signals to use as a factor for decoding the data. In fact, ***Kim*** affirmatively indicates that the size of the data is not used for any type of decoding purposes. As noted above, the Examiner

had indicated that this element is not disclosed or made obvious by ***McKaughan***. Therefore, ***Kim*** does not provide subject matter that makes obvious any element that is also not make obvious by ***McKaughan***. Accordingly, the combination of ***Kim*** and ***McKaughan*** does not make obvious all of the elements of claim 1 of the present invention. Further independent claims 23, 32, and 34 also call for various method and apparatus limitations similar to the subject matter described above. The arguments relating to claim 1 also apply to claims 23, 32, and 34. Therefore, all of the elements of independent claim 1, 23, 32, and 34 are not made obvious by ***Kim, McKaughan***, or their combination and thus, claims 1, 23, 32, and 34 are allowable for at least the reasons cited herein.

Independent claims 1, 23, 32 and 34 are allowable for at least the reasons cited herein. Additionally, dependent claims 2-9, 24-31, and 35, which respectively depend from independent claims 1, 23, and 34 are also allowable for at least the reasons cited herein.

Further, without using improper hindsight reasoning, those skilled in the art would not combine ***Kim*** and ***McKaughan*** in such a manner as claimed by the present application. Appellants respectfully assert that ***McKaughan***, ***Kim***, and/or their combination do not teach or disclose all of the elements of claims 1, 23, 32, and 34 of the present invention. In order to establish a prima facie case of obviousness, the Examiner must consider the following factors: 1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the teachings; 2) there must be a reasonable expectation of success; and 3) the prior art reference(s) must teach or suggest all the claim limitations. MPEP § 2143 (2005) (citing *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). In making an obviousness rejection, it is necessary for the Examiner to identify the reason why a person of ordinary skill in the art would have combined the prior art references in the manner set forth in the claims. *KSR Int'l Co.*

v. Teleflex, Inc., at 14, No. 04-1350 (U.S. 2007). Appellants respectfully submit that the Examiner has not met this burden. If fact, as illustrated herein, ***McKaughan*** and ***Kim*** are incompatible, and consequently those skilled in art would not combine them and make all of the elements of claims of the present invention obvious. Accordingly, Appellants respectfully submit that a *prima facie* case of obviousness has not been established in rejecting claims 1-2, 9, 23-24, 31-32 34 and 35.

McKaughan refers to a computer network that contains a plurality of interconnected computers, wherein a network interface card of sleeping computers detects an incoming packet and compares the incoming packet to a list of packets stored on the network interface cards. In contrast ***Kim*** is directed to performing a pattern matching function. ***Kim*** does not even mention the terms sleep or sleep mode. The Examiner uses improper hindsight reasoning to combine ***McKaughan*** and ***Kim*** in the manner set forth in the claims. Further, the Examiner failed to identify any reason why those skilled in the art would combine ***McKaughan*** and ***Kim*** in the manner set forth in the claims. *KSR Int'l Co. v. Teleflex, Inc.*, at 14. Accordingly, the Examiner failed to establish a *prima facie* case of obviousness has not been established in rejecting claims 1-2, 9, 23-24, 31-32 34 and 35. Therefore, claims 1-2, 9, 23-24, 31-32 34 and 35 are allowable for at least the reasons cited herein.

B. Claims 3-6, 8, 10-18, 20-22, 25-28, 30, 33 and 35 Are Not Rendered Unpatentable under 35 U.S.C. § 103(a) by *McKaughan* (U.S. Patent No. 5,802,305) in view of *Kim* (U.S. Patent No. 5,748,688) and further in view of *Warren* (US 4,516,201)

Contrary to the Examiner's assertions in the Final Office Action, the combination of ***McKaughan*** and ***Kim*** do not teach, disclose or suggest all of the elements of the independent claims of the present invention, from which claims 3-6, 8, 10-18, 20-22, 25-28, 30, 33 and 35 respectively depend. Moreover, the deficit of ***McKaughan*** and ***Kim*** are not made up for by

Warren. Appellant respectfully asserts that even with the use of ***Warren,*** the combination of ***McKaughan, Warren*** and ***Kim*** would still not disclose all of the elements of claims of the present invention.

Warren fails to teach or suggest the subject matter that is not provided by ***McKaughan*** and ***Kim*** in order for there to be a viable argument to suggest obviousness of the above-referenced claims. For example, ***Warren*** discloses a host 12 that passes data transmitted by a data link 14, which is examined by a controller 10. *See* ***Warren***, col. 6, lines 25-36. However, the system disclosed by ***Warren*** does not check for the size of the data signals; it merely converts the received signal from parallel to a serial format. *See* ***Warren***, col. 6, lines 25-36. ***Warren*** merely discloses a link 14 that presents the serial string as parallel words to the host 12. *See* ***Warren***, col. 6, lines 37-48. ***Warren*** discloses status information regarding the data link 14 being provided to the host 12 to take action, however ***Warren*** does not disclose any status information regarding the size of the received data signal as called for by the claims of the present invention.

The only reference to memory size in ***Warren*** relates to the limitation of the host system. ***Warren*** discloses that the host system may be joined via the controller where memory size, data handling capacity, or speed limitations would otherwise preclude their joining to a data link 14. *See* ***Warren***, col. 7, lines 7-17. However, this does not relate to receiving data signals and detecting the size of the received signals and performing the coding and various other steps for waking up a host circuitry as called for by the claims of the present invention.

Warren does not disclose a wake-up sequence called for by the claims of the present invention. ***Warren*** is generally directed towards the data communication link such as a modem providing a queue for data in a controller. This is vastly different from the disclosure of ***McKaughan***, which is directed towards a wake-up sequence. Therefore, without impermissible

hindsight, one of ordinary skill in the art would not combine the disclosure of ***McKaughan*** and ***Warren*** to make obvious any of the claims of the present invention. Therefore, it would be improper hindsight to combine the teachings of ***Warren*** with ***McKaughan*** to make obvious any claim of the present invention. However, even if ***McKaughan***, ***Kim***, and ***Warren*** were combined, as described above, the deficits of ***McKaughan*** are not made up for by ***Warren*** or ***Kim***; including the fact that neither ***McKaughan, Kim***, ***Warren***, nor their combination disclose or make obvious detecting the size of the received set of data signals in the context of decoding the receiving signals, and waking up the host circuitry from a sleep mode, as called for by the claims of the present invention.

For at least the reasons cite above, combining ***Warren***, with the disclosure of ***Kim*** and/or ***McKaughan***, would still not result in disclosing or making obvious all of the elements of any of the claims of the present invention. Therefore, claims 3-6, 8, 10-18, 20-22, 25-28, 30, 33, and 35, are not taught, disclosed, or made obvious by ***McKaughan***, ***Kim***, ***Warren***, or their combinations. Accordingly, claims 3-6, 8, 10-18, 20-22, 25-28, 30, 33, and 35 are allowable for at least the reasons cited above.

Appellant respectfully asserts that it is impermissible hindsight that the Examiner erred because the Examiner's reasoning is not based upon knowledge that was available to those skilled in the art without having read the present disclosure. ***Warren*** is directed towards data communication link whereas ***McKaughan*** is directed towards a wake up sequence. There is no disclosure in ***McKaughan*** and ***Warren*** that would prompt those skilled in the art to combine them to make obvious all of the elements of claims of the present invention. The Examiner does not provide sufficient evidence to support or point to any disclosure in either ***Warren*** or ***McKaughan*** that would direct one skilled in the art to combine them to make obvious all of the elements of claims of the present invention. Again, the Examiner has failed to identify the

reason why those skilled in the art would have combined ***Warren*** with ***McKaughan*** and/or ***Kim*** in the manner set forth in the claims. *KSR Int'l Co. v. Teleflex, Inc.*, at 14. Appellant maintains that those skilled in the art, without using impermissible hindsight reasoning, would not combine ***Warren***, ***McKaughan*** and/or ***Kim*** to make obvious any of the claims of the present invention. Further, as described above, ***McKaughan*** and ***Kim*** are not compatible in the manner used by the Examiner to reject that claims of the present application. Hence, there is insufficient evidence to support any contention that any suggestion or motivation exists to prompt one of ordinary skill in the art to modify the reference or to combine reference teachings, which is a requirement to show a *prima facie* case of obviousness. *In re Vaeck*, 947 F.2d 488; *KSR Int'l Co. v. Teleflex, Inc.*, at 14. Further, as described above, ***McKaughan***, ***Kim***, and ***Warren***, alone or when combined, do not teach or suggest all the claim limitations, which is a requirement to establish a *prima facie* case of obviousness. *Id.* Accordingly, the Examiner erred in maintaining the rejections of claims 3-6, 8, 10-18, 20-22, 25-28, 30, 33 and 35 of the present application. Accordingly, claims 1-35 are allowable for at least the reasons cited herein.

Further, the Examiner had indicated that claims 7, 19 and 29 contain allowable subject matter. Appellant asserts that the Examiner is correct in this assertion, and the Appellant respectfully request that the Board sustain the Examiner's holding that claims 7, 19, and 29 contain allowable subject matter.

Appellant respectfully asserts that the Examiner erred in maintaining the rejection of claim 1-6, 8-18, 20-28, and 30-35, and in light of the arguments provided herein, the Examiner's rejection should be reversed and claims 1-35 should be held to be allowable.

VIII. CLAIMS APPENDIX

The claims currently under consideration, *i.e.*, claims 1-35, are listed in the Claims Appendix submitted herewith.

IX. EVIDENCE APPENDIX

There is no evidence relied upon in this Appeal with respect to this section.

X. RELATED PROCEEDINGS APPENDIX

There are no related appeals and interferences that may affect the outcome of this proceeding.

In view of the foregoing, it is respectfully submitted that the Examiner erred in not allowing all claims (claims 1-35) pending in the present application over the prior art of record.

Reconsideration of the present application is respectfully requested.

In light of the arguments presented above, a Notice of Allowance is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, **the Examiner is requested to call the undersigned attorney** at the Houston, Texas telephone number (713) 934-4069 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

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CLAIMS APPENDIX

1. (Previously Presented) A method for detecting and decoding data comprising:

receiving a set of data signals from an external data source;

detecting a size of said received set of data signals to use as a factor for decoding said data;

decoding said received set of data signals;

extracting a destination address from said set of data signals;

comparing said destination address extracted from said data signals to a known data value;

determining whether said received data signals should be received by a host circuitry based upon said comparison of said destination address extracted from said data signals to said known data value;

generating at least one status signal alerting said host circuitry of said determination that said received data signals should be received by said host circuitry; and

waking up said host circuitry from a sleep mode upon a determination that said received set of data is addressed to said host circuitry.

2. (Original) The method as described in claim 1, wherein said set of data signal received is a data packet that is in a serial data format, over a network line.

3. (Previously Presented) The method as described in claim 2, further comprising detecting said size of said received set of data signal and decoding said received set of data signals, detecting and decoding said size of said received set of data signal comprising:

converting a serial data packet into a parallel data format;

extracting a word clock from a received data packet;

incrementing a number held by a counter, said word clock generating a word count;

inputting said converted parallel format data into a plurality of comparators;

using said word count to address data stored in a memory circuitry; and

inputting a set of data signals from said memory circuitry into an appropriate comparator.

4. (Previously Presented) The method as described in claim 3, wherein said act of extracting said destination address from said set of data signals further comprises slicing said parallel data such that at least one destination address data word is generated.

5. (Previously Presented) The method as described in claim 3, wherein said method of comparing said destination address to a known data value further comprises:

performing a comparison function upon said converted parallel set of data signals and said set of data from said memory circuitry;

generating a digital comparator status signal in response of said performance of comparator function; and

clocking in said digital comparator data signal into a register.

6. (Previously Presented) The method as described in claim 5, wherein said method of determining whether said received data signals should be received by said host circuitry further comprises latching all output of said plurality of comparators into a digital logic circuitry.

7. (Original) The method as described in claim 6, wherein said output of said comparators are not latched when a mask circuitry indicates that a particular frame of data is not compared.

8. (Original) The method as described in claim 5, wherein said method of generating a status signal alerting said host circuitry further comprises performing an OR function upon all said latched output of said comparators.

9. (Previously Presented) The method as described in claim 1, wherein said method of waking up said host circuitry further comprises generating a status signal alerting said host circuitry that a address match has been found.

10. (Previously Presented) An apparatus for detecting and decoding data, comprising:

means for receiving a data signal;

means for detecting a size of said received data signal;

a data formatter;

a clock divider;

a counter;

a host circuitry interface capable of transmitting and receiving data from a host circuitry, said host circuitry enter a wake up state from a sleep mode based upon decoded address data received by said host circuitry, said decoded address data being based_upon a content of_said data signal and said size of said received data signals;

a memory circuitry;

a plurality of comparators;

a mask circuitry;

a digital logic circuitry;

a plurality of status registers; and

a plurality of clocked registers.

11. (Original) The apparatus as described in claim 10, wherein said data formatter comprises of a serial to parallel converter and a data end detector that are capable of converting a serial stream of data into parallel data words and detecting an end of a data stream.

12. (Original) The apparatus as described in claim 10, wherein said clock divider is capable of incrementing a count held by said counter.

13. (Original) The apparatus as described in claim 10, wherein said memory circuitry comprises of a memory element and a memory data access logic.

14. (Original) The apparatus as described in claim 13, wherein said memory element is coupled with said memory data access logic such that data from said memory element can be retrieved and sent through said memory data access logic.

15. (Original) The apparatus as described in claim 14, wherein said memory data access logic is coupled with said host interface such that data can be sent to and retrieved from said memory elements.

16. (Original) The apparatus as described in claim 10, wherein said comparators are coupled with said data formatter such that said comparators receive parallel formatted data from said data formatter.

17. (Original) The apparatus as described in claim 16, wherein said comparators are further coupled with said memory circuitry such that said comparator is capable of receiving data from said memory circuitry.

18. (Original) The apparatus as described in claim 17, wherein at least one output from said comparators is further coupled to said digital logic circuitry and said clock registers such that said output of said comparators is latched by said digital logic circuitry and said clock registers.

19. (Original) The apparatus as described in claim 18, wherein said mask circuitry is capable of preventing a registering of said comparator output into said clocked registers.

20. (Original) The apparatus as described in claim 18, wherein said status registers are coupled to said digital logic circuitry and said clocked registers such that said latched comparator outputs are inputted into said status registers.

21. (Original) The apparatus as described in claim 10, wherein an output from said digital logic circuitry is clock-registered by a signal output from said data formatter.

22. (Previously Presented) The apparatus as described in claim 10, wherein said status registers are coupled with said host interface such that data from said status register could be retrieved through an access port.

23. (Previously Presented) A computer readable program storage device encoded with instructions that, when executed by a computer, performs a method, comprising:

receiving a set of data signals from an external data source;

detecting a size of said received set of data signals to use as a factor for decoding said data signals;

decoding said received set of data signals;

extracting a destination address from said set of data signals;

comparing said destination address extracted from said data signals to a known data value;

determining whether said received data signals should be received by a host circuitry based upon said comparison of said destination address extracted from said data signals to said known data value;

generating at least one status signal alerting said host circuitry of said determination that said received data signals should be received by said host circuitry; and

waking up said host circuitry from a sleep mode upon a determination that said received set of data is addressed to said host circuitry.

24. (Previously Presented) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 23, wherein said set of data signal received is a data packet that is in a serial data format, over a network line.

25. (Previously Presented) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 24, further comprising detecting said size of said received set of data signal and decoding said received set of data signals, detecting and decoding said size of said received set of data signal comprising:

converting said serial data packet into a parallel data format;

extracting a word clock from said received data packet;

incrementing a number held by said counter, said word clock generating a word count;

inputting said converted parallel format data into a plurality of comparators;

using said word count to address data stored in a memory circuitry; and

inputting a set of data signals from said memory circuitry into an appropriate comparator.

26. (Previously Presented) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 25, wherein said act of extracting said destination address from said set of data signals further

comprises slicing said parallel data such that at least one destination address data word is generated.

27. (Previously Presented) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 25, wherein said method of comparing said destination address to said known data value further comprises:

performing a comparison function upon said converted, parallel set of data signals, and said set of data from said memory circuitry;

generating a digital comparator status signal in response of said performance of comparator function; and

clocking in said digital comparator data signal into a register.

28. (Previously Presented) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 27, wherein said method of determining whether said received data signals should be received by said host circuitry further comprises latching all output of said plurality of comparators into a digital logic circuitry.

29. (Previously Presented) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 28, wherein said output of said comparators are not latched when a mask circuitry indicates that a particular frame of data is not compared.

30. (Previously Presented) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 28, wherein said method of generating a status signal alerting said host circuitry further comprises performing an OR function upon all said latched output of said comparators.

31. (Previously Presented) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 23, wherein said method of waking up said host circuitry further comprises generating a status signal alerting said host circuitry that a address match has been found.

32. (Previously Presented) A method, comprising:

receiving a data signal;

detecting a size of said received data signal to use as a factor for extracting a destination address;

extracting said destination address based upon said data signal to determine whether a host circuitry is being addressed by comparing said destination address to a predetermined address; and

waking up said host circuitry from a sleep mode based upon said determination that said host circuitry is being addressed.

33. (Previously Presented) The method of claim 32, wherein extracting said destination address further comprises:

converting a serial data packet from said received data into a parallel data format;

extracting a word clock from said received data packet;

incrementing a number held by a counter, said word clock generating a word count;

inputting said converted parallel format data into a plurality of comparators;

using said word count to address data stored in a memory circuitry;

inputting a set of data signals from said memory circuitry into an appropriate comparator; and

extracting said destination address by slicing said parallel data such that at least one destination address data word is generated.

34. (Previously Presented) An apparatus, comprising a controller to:

receive a data signal;

detect a size of said received set of data signals to use as a factor to extract a destination address;

extract said destination address based upon said data signal to determine whether a host circuitry is being addressed by comparing said destination address to a predetermined address; and

wake up said host circuitry from a sleep mode based upon said determination that said host circuitry is being addressed.

35. (Previously Presented) The apparatus of claim 34, further comprising:

a data formatter capable of converting a serial stream of data into parallel data words and detecting an end of a data stream;

a counter to receive parallel formatted data from said data formatter;

a clock divider capable of incrementing a count held by a counter;

a memory circuitry comprising a memory element and a memory data access logic;

a plurality of comparators to receive parallel formatted data from said data formatter;

a plurality of clocked registers;

a mask circuitry capable of preventing a registering of said comparator output into said clocked registers; and

a plurality of status registers to latch an output from said comparators.